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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN L. PLINE, KENNETH KAY SMITH,
COLIN ANDREW STOBBS, STEWART WYATT,
DAVID MURRAY BANKS, ROBIN ALEXIS TAKASUGI, and
DAVID MCINTYRE

Appeal 2008-004596
Application 10/725,855
Technology Center 2100

Decided: September 23, 2009

Before JOSEPH L. DIXON, ST. JOHN COURTENAY III, and
THU A. DANG, *Administrative Patent Judges*.

DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1-35. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

A. INVENTION

The invention at issue on appeal provides a magnetic memory data storage and retrieval system operable on a host computer. The system comprises a sparing system configured to replace defective memory sections of a magnetic memory device with replacement memory sections of the magnetic memory device, and an error correction code system. The error correction code system is configured to encode data with an error correction code to store the data into the magnetic memory device and decode the encoded data with the error correction code to retrieve the data from the magnetic memory device. (Spec. 3.)

B. ILLUSTRATIVE CLAIM

Claim 1, which further illustrates the invention, follows.

> 1. A data storage and retrieval system operating on a host computer, the data storage and retrieval system comprising:
>
> a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the

memory device, the sparing system comprising computer readable instructions stored in a host memory of the host computer; and

an error correction code system configured to encode data with an error correction code, store the data into the memory device, and decode the encoded data with the error correction code to retrieve the data from the memory device, the error correction code system comprising computer readable instructions stored in the host memory of the host computer.

C. REFERENCES

The Examiner relies on the following references as evidence:

Weng	US 5,428,630	Jun. 27, 1995
Buternowsky	US 5,809,090	Sep. 15, 1998
Hiratsuka	US 6,119,245	Sep. 12, 2000
Tsunoda	US 2003/0028733 A1	Feb. 6, 2003
Kleveland	US 20030115518 A1	Jun. 19, 2003

Riley, Martyn, Reed-Solomon codes, Aug 2, 2002, http://www.4i2i.com/reed_solomon_codes.htm, Pages 1-2

D. REJECTIONS

Claims 1-8, 10, 11, 13-17, 23 and 26-35 are rejected under 35 U.S.C. 102(b) as being unpatentable by Hiratsuka.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Martyn Riley.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Weng.

Claims 18, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Tsunoda.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratysuka taken in view of Kleveland.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Buternowsky.

II. ISSUE

Have Appellants shown error in the Examiner's initial showing of anticipation? Specifically, have Appellants shown that the Examiner's interpretation that the teachings of Hiratsuka are within a "host system" to be unreasonable?

III. PRINCIPLES OF LAW

35 U.S.C. § 102

"[A]nticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim . . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.,* 730 F.2d 1452, 1457 (Fed. Cir. 1984)). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.,* 793 F.2d 1565, 1571 (Fed. Cir. 1986).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

Appellants have the opportunity on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted).

IV. ANALYSIS

With respect to independent claim 1, Appellants' main contention is that Hiratsuka discloses a disk controller which includes a host interface 121 for communicating with a host computer and that the host computer in Hiratsuka does not perform any of the error correction, data error

information management, or address conversion functions. The host computer in Hiratsuka provides command information and address information to semi-conductor device 100 through host interface 121. (App. Br. 7-8). Appellants contend that the "address conversion and the ECC functions disclosed by Hiratsuka are performed independently from the host computer and without the host computer's knowledge. The host computer just reads and writes data to the memory device 100 without being involved in the address conversion or ECC functions." *Id. at 8.* Appellants argue that "the sparing system and the error correction code systems recited by claim 1 are implementing using computer readable instructions executed on the host computer. The host computer performs the sparing and ECC functions. The memory device recited by claim 1 has no knowledge or control of the sparing system or the ECC system." *Id.* We find Appellants' argument is not commensurate in scope with the express language of independent claim 1. Therefore, Appellants' argument is not persuasive of error in the Examiner's initial showing of anticipation.

At page 20 of the Answer to the Examiner maintains:

> As stated in the final rejection the disk device section (Figure 1.100) is part of the "host system" as applicants "host memory" shown in figure 1.28 is considered part of "host system". Hiratsuka discloses a semiconductor storage device that is directly interfaced with a host (Figure 1, column 5, lines 20-23). The semiconductor storage device is part of your host computer the same way a hard drive is part of your desktop computer. Hiratsuka does not disclose the semiconductor storage device being accessed over a network, nor does Hiratsuka disclose the semiconductor storage device being accessed by multiple

> computers. Since program memory 132 stores the computer readable instructions for performing the functions of the sparing system and the error correction code system and the memory 132 is located on the "host system" the host does in fact have knowledge and control of the functions being performed (column 6, lines 30-36).

We agree with the Examiner's position and find that the recited claim limitations/functions are taught by Hiratsuka. The language of independent claim 1 sets forth in the preamble "data storage and retrieval system operating on a host computer" (emphasis added) and later in the body of the claim recites "computer readable instructions stored in a host memory of the host computer" and "computer readable instructions stored in the host memory of the host computer" (emphasis added).

We find no express limitation recited in the language of independent claim 1 which identifies or details the "host computer" or "host memory." Because the storage device of Hiratsuka is connected to a host system as shown in figure 1, we agree with the Examiner's line of reasoning that system 100 may be deemed to be part of a "host system" and "host memory." Therefore, we find the Examiner's position to be reasonable. Since Appellants have shown no error in the Examiner's initial showing of anticipation of independent claim 1, we will sustain rejection thereof and its respective dependent claims.

With respect to independent claims 13, 23, 29, and 33 and their respective dependent claims, Appellants reiterate the language of the claims and assert that for the reasons set forth with respect to claim 1, Hiratsuka does not anticipate the claimed inventions, nor does Hiratsuka render obvious the claimed invention in combination with the secondary references

applied. We find Appellants' arguments do not rise to the level of separate arguments for patentability, and we will group these claims as standing or falling with independent claim 1. *See* 37 C.F.R. § 41.37(c)(1)(vii).

VI. CONCLUSION

Appellants have shown no error in the Examiner's initial showing of anticipation and have not shown that the Examiner's interpretation that the teachings of Hiratsuka are within a "host system" to be unreasonable in light of the broad language of independent claim 1.

VII. ORDER

We affirm the anticipation rejection of claims 1-8, 10, 11, 13-17, 23 and 26-35, and we affirm the obviousness rejections of claims 9, 12, 18-22, 24, and 25.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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